itself, however, in respect of its structure, construction and lay-out, as well as manufacturing techniques, together with other objects and advantages thereof, will be best understood from the following description when read with reference to the drawing.–;

line 20: insert –DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT.–;

Page 5, line 1: cancel "Patent Claims" and substitute –What is claimed is:– therefor;

page 9, line 1: cancel "Abstract" and substitute –ABSTRACT OF THE DISCLOSURE.– therefor;

lines 3 and 4: cancel;

line 5: cancel "this purpose, the invention provides a" and substitute –A– therefore and cancel "which";

line 6: cancel "comprises" and substitute –having– therefor;

line 7: cancel ". The"

line 8: cancel "inventive transistor is characterized in that" and substitute –,– therefor and change "is" to –being–;

line 11: cancel "and" (first occurrence) and substitute --,-- therefor;

line 12: change "are" to --being--, change "and" to –,–, and change "is" to –being–.

In the claims:

Cancel claim 1 and substitute the following new claim:

23. (New) A vertical nano-transistor, comprising:

a source region;

a drain region;

a semiconductor channel region intermediate the source region and the drain region;

a gate region comprising a metal film, the transistor being embedded in the metal film such that the gate region and the semiconductor channel region form a coaxial structure and the source region, the semiconductor channel region and the drain region being vertically arranged; and

the gate region being electrically insulated from the source region, the drain region and the semiconductor channel region.

Claim 2, line 1: change "1" to for forming

a metal layer on the flexible insulating substrate and on an upper portion of the channel region for forming a gate region;

the cylindrical channel region being enclosed by the gate region such that the gate region and the upper channel portion form a coaxial structure; and

an electrical insulation between the gate region and the source contact, the drain contact and the semiconductor channel region and on the upper and lower surfaces of the flexible insulating substrate.

Claim 2, line 1: change "1" to –23;

line 2: cancel; "(3)";

claim 3, line 1: change "1" to –23;

line 2: cancel "G)";

line 3: cancel "(1);

claim 4, line 1: change "1" to –23;

line 2: cancel "(3)";

claim 5, line 1: change "1" to –23;

line 2: cancel "(2)";

line 3: cancel "(G)" and "(3)";

claim 6, line 1: change "1" to –23;

line 2: cancel "(2)";

line 3: cancel "(1)";

Amend claims 7 and 8 as follows:

7. (Currently amended) The transistor of claim 23,

wherein the semiconductor channel comprises a material selected from the group consisting of CuSCN, TiO_2, PbS, ZnO and another compound semiconductor.

8. (Currently amended) The transistor of claim 23,
wherein the source and the drain comprise a material selected from the group consisting of Au, Ag, Cu, Ni and Al.

Claim 9, line 1: change "1" to –23–;
line 2: cancel "(S)" and "(D)".

Amend claim 10 as follows:
10. (Currently amended) A memory arrangement, comprising:
a metal foil; and
a plurality of transistors according to claim 23 arranged adjacent each other within the metal film.

Claim 11, line 3: cancel "(4)", "(1)" and "(G)";
line 4: cancel "(3)";
line 5: cancel "(4)";
line 7: cancel "(1)";
line 8: cancel "(4)";
line 9: cancel "(3)";
line 10: cancel "(S)" and "(D)";

claim 12, line 2: cancel "(4)" and "(1)";
claim 13, line 2: cancel "(4)" and "(1)";
claim 14, line 3: cancel "(1)";
claim 15, line 2: cancel "(4)";
line 3: cancel "(1)";
claim 16, line 2: cancel "(4)";
line 3: cancel "(1)";
claim 17, line 2: cancel "(4)";
line 3: cancel "(1)";

Amend claim 18 as follows: